차세대 집적회로 연구실 (ICE)
Integrated Circuits for Emerging Tech.

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01 연구실구성원

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- 석사과정 : 윤지형, 이하연
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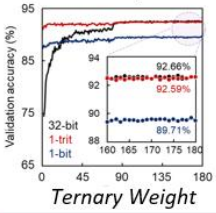
02 연구분야

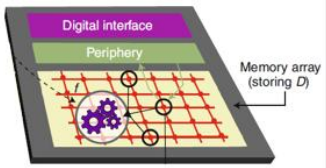
차세대 집적회로 연구실(ICE)은 Emerging tech.를 위한 집적회로(IC)를 연구합니다. 우리는 post Moore's law 시대에서, device scaling을 이을 다음 패러다임을 찾고 있습니다. 그 중 소자 크기의 한계를 넘어 본질적인 수를 줄일 수 있는 logical scaling에 주목합니다. 첫 단계인 삼진법 반도체, 그 가능성을 검증하기 위해 우리는 다수의 회로 설계 IP와 대규모 집적을 위한 설계 자동화 SW를 개발했습니다. 시스템 수준 연구로 나아가며, 열정적인 학생들과 함께 가장 창의적인 연구로써 압도적인 결과물을 보이고자 합니다.

PIM 기반 AI Chip 설계

- **HW/SW co-design** of a PIM AI chip using **emerging tech.** to optimize the accuracy-energy trade-off.



Ternary Weight

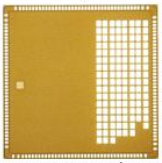


PIM Architecture

시스템 반도체 (SoC) 설계

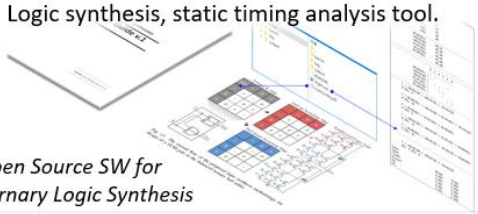
- **HW development** with **Very-Large-Scale Integration (VLSI)** of emerging technology.
- CPU ASIC physical design (RTL-to-GDS, auto P&R)

Test Board (PCB)


Ternary CPU (ASIC)

VLSI 설계 자동화 (CAD)

- **SW development** for **electronic design automation (EDA)** of emerging technology.
- Logic synthesis, static timing analysis tool.


Open Source SW for Ternary Logic Synthesis

수행과제

- **National Research Foundation**
  - *Nano Material Technology Development (current)*
  - *Memcapacitor-based MVL architecture ('17-'23)*
  - *MVL device integration platform ('19-'21)*
  - *Graphene-based ternary logic architecture ('16-'21)*
- **Samsung Research Funding & Incubation Center**
  - *2D semiconductor-based ternary circuits ('20-'22)*
  - *Ternary CMOS-based Neural Net IC Design ('17-'18)*

03 최근 5년간 연구 논문

❑ International Journal

- Optimizing Ternary Multiplier Design with Fast Ternary Adder, IEEE Transactions on Circuits and Systems II: Express Briefs, 2022.
- Demonstration of Anti-ambipolar Switch and Its Applications for Extremely Low Power Ternary Logic Circuits, ACS Nano, 2022.
- Low-power Ternary Multiplication Using Approximate Computing, IEEE Transactions on Circuits and Systems II: Express Briefs, 2021.
- A Logic Synthesis Methodology for Low-Power Ternary Logic Circuits, IEEE Transactions on Circuits and Systems I: Regular Papers, 2020.
- Tunneling-Based Ternary Metal-Oxide-Semiconductor Technology for Digital Paradigm Shift, Nature Electronics, 2019.
- Ternary Full Adder Using Multi-Threshold Voltage Graphene Barristors, IEEE Electron Device Letters, 2018.

❑ International Conference

- Design and Evaluation Frameworks for Advanced RISC-based Ternary Processor, IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE), 2022.
- Memcapacitor based Minimum and Maximum Gate Design, IEEE International SoC Design Conference (ISOCC), 2021.
- Ternary Sense Amplifier Design for Ternary SRAM, IEEE International SoC Design Conference (ISOCC), 2021.
- Design and Analysis of a Low-Power Ternary SRAM, IEEE International Symposium on Circuits and Systems (ISCAS), 2021.
- MTCMOS-based Ternary to Binary Converter, IEEE International SoC Design Conference (ISOCC), 2020.
- Low-power 4-trit Current-steering DAC for Ternary Data Conversion, IEEE International SoC Design Conference (ISOCC), 2020.
- Extreme Low Power Technology Using Ternary Arithmetic Logic Circuits via Drastic Interconnect Length Reduction, IEEE International Symposium on Multiple-Valued Logic (ISMVL), 2020.
- Multi-Threshold Voltages Graphene Barristor-Based Ternary ALU, IEEE International SoC Design Conference (ISOCC), 2019.
- Design of Quad-Edge-Triggered Sequential Logic Circuits for Ternary Logic, IEEE International Symposium on Multiple-Valued Logic (ISMVL), 2019.
- Ternary Logic Synthesis with Modified Quine-McCluskey Algorithm, IEEE International Symposium on Multiple-Valued Logic (ISMVL), 2019.
- Multi-threshold graphene barristor for standard ternary inverter, International Conference on Electronic Materials and Nanotechnology for Green Environment (ENGE), 2018.
- An Optimal Gate Design for the Synthesis of Ternary Logic Circuits, IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC), 2018.

04 특허 및 등록출원 현황

❑ **국제특허 출원 및 등록**

- INVERTER INCLUDING TRANSISTORS HAVING DIFFERENT THRESHOLD VOLTAGES AND MEMORY CELL INCLUDING THE SAME, US 18/060,223 (출원).
- TERNARY LOGIC CIRCUIT DEVICE, US 17/489,629 (출원).
- TERNARY LOGIC CIRCUIT DEVICE, US 17/489,624 (등록).
- APPARATUS FOR LOW POWER TERNARY LOGIC CIRCUIT, US 17/175,570 (등록).
- APPARATUS AND METHOD FOR TERNARY LOGIC SYNTHESIS WITH MODIFIED QUINE-MCCLUSKEY ALGORITHM, US 16/714,583 (등록).

❑ **국내특허 출원 및 등록**

- 다른 문턱 전압들을 갖는 트랜지스터들을 포함하는 인버터 및 이를 포함하는 메모리 셀, KR 10-2022-0134349 (출원).
- 삼진 곱셈기, KR 10-2021-0131932 (출원).
- 삼진-이진 변환기 및 이의 삼진-이진 변환 방법, 및 이진-삼진 변환기 및 이의 이진-삼진 변환 방법, KR 10-2568174 (등록).
- 삼진 논리 회로 장치, KR 10-2505200 (등록).
- 삼진 논리 회로 장치, KR 10-2505205 (등록).
- 저전력 삼진 논리 회로 장치, KR 10-2348169 (등록).
- 변조 퀸맥클러스키 알고리즘을 이용한 삼진 논리 합성 장치 및 방법, KR 10-2130980 (등록).
- 삼진 순차 회로 장치, KR 10-1991622 (등록).
- 삼진 논리 회로 장치, KR 10-1928223 (등록).