Mobile SOC and Microprocessor Lab.

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01 연구실구성원

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02 연구실 소개

The main research area of our lab includes computer architecture, microprocessor, and system-on-chip (SOC) design, and hardware security. These research topics are being actively studied in the industry as well as academia.

03 연구분야

❑ **Mobile AP design**

- Energy-efficient, high-performance, and low cost mobile AP design
  : 모바일 AP 및 SOC는 최근 아주 널리 사용되고 있는 모바일 시스템 구성 회로임
  : 본 연구실에서는 모바일 AP 및 SOC 설계에 있어 에너지, 성능, 비용 측면에서 가장 최적화된 mobile AP 및 SOC를 설계하고자 함
- Future mobile system architecture design
  : 모바일 시스템을 구성하는 메모리 서브시스템 및 통신용 프로세서와의 co-optimization을 통해 전체 모바일 시스템의 에너지 측면 최적화 및 성능 향상에 대한 연구를 수행함
- Thermal management for mobile systems and APs
  : 온도 문제는 모바일 시스템의 성능을 저하시키고 전력 효율성을 저하시키는 중요한 문제임
  : 이러한 문제를 극복하기 위하여 모바일 시스템에서의 온도 최적화를 통해 성능 및 전력 효율성을 향상시키는 연구를 수행함
- Architecture exploration with emerging memory cells
  : STT-RAM과 같은 최신 메모리 셀을 이용한 효율적인 모바일 시스템 구조를 개발함

❑ **Next-generation processor and memory subsystem architecture design**

- 3D-die stacked processor architecture
  : 3차원으로 프로세서 다이(die)를 적층하여 에너지 소모를 줄이고 성능을 높임
  : 3차원 구조에서 심각한 온도 문제를 해결하기 위해 구조적인 기법 연구
- 3D-die stacked memory subsystem architecture
  : 메모리 다이를 3차원 적층구조로 쌓은 메모리 구조가 최근 차세대 메모리 구조로 떠오름
  : Wide-IO, HMC (hybrid memory cude), HBM (high bandwidth memory) 등의 연구와 더불어 시스템 전체적인 성능과 에너지 효율성을 높이는 기법을 개발

❑ **Reliable and cost-effective microprocessor design**

- Process variation-aware processor architecture design

: 공정변이는 소자의 크기가 작아질수록 프로세서의 성능, 에너지 효율성 및 비용 측면에서 악영향을 줌
: 공정변이를 고려한 프로세서 구조 설계 및 수율을 높이기 위한 연구 수행

- Process variation-aware and cost-effective near-threshold computing
: 에너지 효율성을 높이기 위한 near-threshold computing(NTC)은 공정변이에 더욱 더 취약함
: NTC에서 에너지 효율적이고 저비용의 캐쉬 메모리 구조를 설계

❑ Physically Unclonable Function (PUF) design for hardware security

- Physically unclonable function design
: 최근 떠오르는 security primitive인 PUF를 활용하여 시스템의 보안을 향상시킴

04 최근 주요 연구 논문

❑ International journal

- **[ELEX – SCIE] Joonho Kong**, "A Novel Technique for Technology-Scalable STT-RAM Based L1 Instruction Cache", IEICE Electronics Express, vol. 13, no. 11, May 2016.
- **[JSTS – SCIE] Joonho Kong**, "A Locality-Aware Write Filter Cache for Energy Reduction of STTRAM-Based L1 Data Cache", Journal of Semiconductor Technology and Science, vol. 16, no. 1, February 2016.
- **[IEEE TC – SCI] Joonho Kong**, Farinaz Koushanfar and Sung Woo Chung, "An energy-efficient last-level cache architecture for process variation-tolerant 3D microprocessors", IEEE Transactions on Computers, vol. 64, no. 9, September 2015.
- **[IEEE TETC] Joonho Kong** and Farinaz Koushanfar, "Processor-Based Strong Physical Unclonable Functions with Aging-Based Response Tuning", IEEE Transactions on emerging topics in computing, vol. 2, no. 1, March 2014.
- **[IEEE TC – SCI]** Hyung Beom Jang, Junhee Lee, **Joonho Kong**, Taeweon Seo, and Sung Woo Chung, "Leveraging Process Variation for Performance and Energy: In the Perspective of Overclocking", IEEE Transactions on Computers, vol. 63, no. 5, May 2014.
- **[ACM TODAES – SCIE]** Mehrdad Majzoobi, **Joonho Kong**, and Farinaz Koushanfar, "Low Power Resource Binding by Post-Silicon Customization", ACM Transactions on Design Automation of Electronic Systems, vol. 18, no. 2, article 26, March 2013.
- **[IEEE TCE – SCI]** Minyong Kim, **Joonho Kong**, and Sung Woo Chung, "Enhancing Online Power Estimation Accuracy for Smartphones", IEEE Transactions on Consumer Electronics, vol. 58, no. 2, pp. 333-339, May 2012.
- **[ACM CSUR – SCI] Joonho Kong**, Sung Woo Chung, and Kevin Skadron, "Recent Thermal Management Techniques for Microprocessors", ACM Computing Surveys, vol. 44, no. 3, article 13, June 2012 (recent 5-year IF: 7.854).
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- **[IEEE COMPUTER – SCI]** Jae Min Kim, Minyong Kim, **Joonho Kong**, Hyung Beom Jang, Sung Woo Chung, "Display Power Management That Detects User Intent", IEEE Computer Magazine, vol. 44, no. 10, pp. 60-66, October 2011.
- **[IET EL – SCI]** Minyong Kim, **Joonho Kong**, Taeweon Suh, and Sung Woo Chung, "Latch-based FPGA Emulation Method for Design Verification: a case study with a microprocessor", IET

Electronics Letters, vol. 47, no. 9, pp. 532-533, April 2011 (also introduced in feature section).

· **[IEEE TDSC – SCIE] Joonho Kong**, Johnsy John, Eui-Young Chung, Sung Woo Chung, and Jie Hu, "On the Thermal Attack in Instruction Caches", IEEE Transactions on Dependable and Secure Computing , vol. 7, no. 2, pp. 217-223, April-June 2010.

❑ **International conference**

· **[GLSVLSI] Joonho Kong**, Arslan Munir, and Farinaz Koushanfar, "Fine-Grained Voltage Boosting for Improving Yield in Near-Threshold Many-Core Processors", ACM Great Lakes Symposium on VLSI, May 2015.

· **[DAC] Joonho Kong**, Christian Wachsmann, Praveen K. Pendyala, Farinaz Koushanfar, and Ahmad-Reza Sadeghi, "PUFatt: Embedded Platform Attestation Based on Novel Processor-Based PUFs", Design Automation Conference (DAC - **Top 15th conference among 3,516 Computer Science conferences**), June 2014, (best paper candidate).

· **[ICICDT]** (Invited paper) **Joonho Kong** and Sung Woo Chung, "Process variation-tolerant 3D microprocessor design: an efficient architectural solution", International Conference on IC Design and Technology (ICICDT), May 2013.

· **[DAC] Joonho Kong** and Sung Woo Chung, "Exploiting Narrow-Width Values for Process Variation-Tolerant 3-D Microprocessors", Design Automation Conference (DAC – **Top 15th conference among 3,516 Computer Science conferences** from Microsoft Academic search), June 2012 (acceptance rate: 164/741= 22.1%).

· **[ICCE]** Minyong Kim, **Joonho Kong**, and Sung Woo Chung, "An Online Power Estimation Technique for Multi-Core Smartphones with Advanced Display Components", The International Conference on Consumer Electronics (ICCE), January 2012.

· **[DAC]** Yan Pan, **Joonho Kong**, Serkan Ozdemir, Gokhan Memik, and Sung Woo Chung, "Selective Wordline Voltage Boosting for Caches to Manage Yield under Process Variations", Design Automation Conference (DAC – **Top 15th conference among 3,516 Computer Science conferences**), July 2009 (acceptance rate: 148/682 = 21.7%).

· **[ICCIT] Joonho Kong**, Jinhang Choi, Lynn Choi, and Sung Woo Chung, "Low-cost Application-aware DVFS for Multi-core Architecture", The International Conference on Convergence and hybrid Information Technology (ICCIT), November 2008.

· **[ITC-CSCC] Joonho Kong**, Eui-Young Chung, and Sung Woo Chung, "Energy-Efficient Soft Error Protection Utilizing Idle Resources", International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC), July 2007.

05 특허 및 등록출원 현황

❑ **국내특허 등록**

· Memory device, processor and data writing/reading method, Korea Registration Number: 1012819710000, June 27, 2013, Korea

· Apparatus and method for scheduling task and resizing cache memory of embedded multicore processor, Korea Registration Number: 1012325610000, February 5, 2013, Korea

· CPU Frequency Selection Device And Method Thereof, Korea Registration Number: 1011044710000, January 3, 2012, Korea.

· Method for managing computer power using web camera, Korea Registration Number: 1010834730000, November 8, 2011, Korea.

· Cache memory, Korea Registration Number: 1010416820000, June 8, 2011, Korea.
· Cache memory, Korea Registration Number: 1009482710000, March 11, 2010, Korea.
· Microprocessor system, Korea Registration Number: 1009757470000, August 6, 2010, Korea.
· Method for preventing damage of instruction cache memory by malicious code, Korea Registration Number: 1009165500000, September 2, 2009, Korea.
· Method for writing data in data bit array of the cache memory including fault data bit and method for reading data from data bit array of the cache memory including fault data bit, Korea Registration Number: 1009045180000, June 17, 2009, Korea.

❑ **국제특허 등록**

· Cache memory, United States Publication Number: US8068381 B2 (grant), November 29, 2011, United States.